

different 6.3Gbit/s channels are clearly observed. The BER performance of the six channels is shown in Fig. 5. Note that the average received optical power is that of the 100Gbit/s signal monitored right after the optical attenuator (see Fig. 2), corresponding to the receiver sensitivity for the 100Gbit/s signal. The baseline 6.3Gbit/s BER curve was measured at 1555nm at the output from the intensity modulator. Fig. 5 shows that simultaneous demultiplexing of the six channels is successfully performed with no error floor. The power penalties range from 3.0 (channel 3) to 5.5dB (channel 1), taking into consideration the subtraction of 12dB, i.e. the OTDM multiplication factor of 16. Fig. 6 shows the characteristics of demultiplexed channel 1 with the wavelength of 1535nm, including the streak camera image (Fig. 6a), the eye-diagram observed after the O/E-converter with 6GHz bandwidth (Fig. 6b), and the output of the electrical decision circuit (Fig. 6c). The demultiplexed signal has a clear eye-opening. The uplift of the 'space' level comes from the spectral power component of the original down-chirped clock at the corresponding wavelength, which simply results in an increase in the decision level.

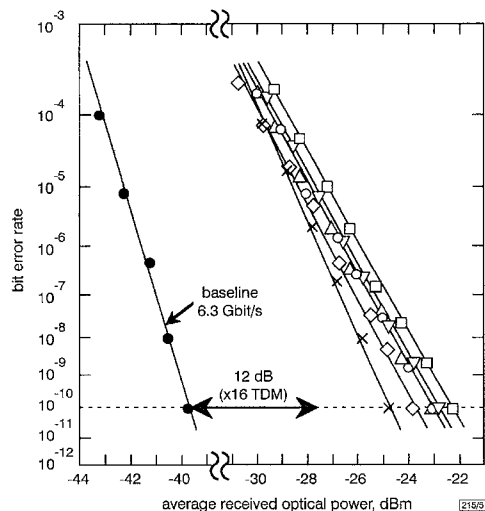


Fig. 5 Bit error rate performance, PRBS $2^{15} - 1$

□ ch1, ○ ch2, × ch3, △ ch4, ◇ ch5, ▽ ch6

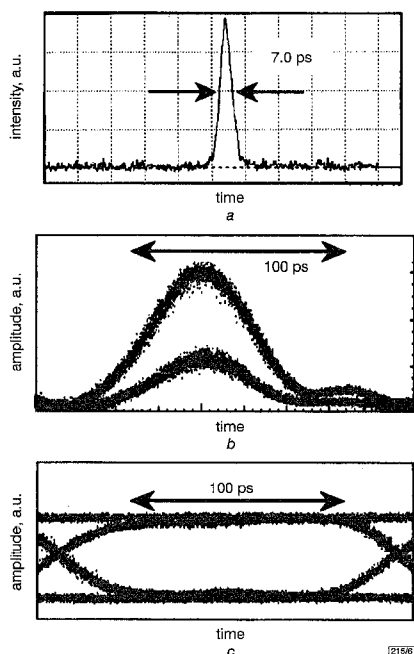


Fig. 6 Characteristics of demultiplexed Ch. 1

a For streak camera image, b For eye-diagram
c For output of decision circuit

Conclusion: We have proposed a novel multiple-channel output all-optical OTDM demultiplexer utilising cross-phase modulation (XPM)-induced chirp compensation (MOXIC). Stable, error-free, simultaneous six-channel-output, 100 to 6.3Gbit/s demultiplexing has been successfully demonstrated by the MOXIC. The MOXIC

does not utilise any parametric process-based wavelength conversion or interferometric switching technique, and, consequently, it has a very simple setup with both low insertion loss and stable operation. It may offer a practical solution to all-optical time-division demultiplexers over 100Gbit/s.

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K. Uchiyama, S. Kawanishi and M. Saruwatari (NTT Optical Network Systems Laboratories, 1-1 Hikarinooka, Yokosuka, Kanagawa, 239 Japan)

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On the odd-even ATM switch

C. Koliass and L. Kleinrock

The authors address some issues with respect to their previously proposed switching architecture the odd-even ATM switch.

System description: We would like to indicate that the work in [1] was anticipated by ours in 1995 and 1996 [3 - 5].

In particular, in [4] we describe the novel idea of an ATM switch where a single input queue is expanded into two separate FIFO queues each able to store incoming cells according to their desired output port. More specifically we let cells that are destined to the even-numbered output ports (i.e. 2, 4, 6, ...) join what we call the even queue while those destined to the odd-numbered output ports (i.e. 1, 3, 5, ...) join, respectively, the odd queue. This type of switching architecture was originally introduced to us by L.G. Roberts and we named it the odd-even ATM switch. The idea of the odd-even switch was first presented in [3]. In [5] we give an approximate throughput analysis of the odd-even model.

We here reproduce some of the key elements and issues of our previously published work on the subject of the odd-even ATM switch [Note 1].

Note 1: Parts of the following text contain a verbatim passage from our papers [4, 5].

